18. Cancelled.

19. Cancelled.

C4

21. (Amended) The gaming machine of claim 10, wherein the first processor on the mother board and the first gaming processing subsystem board communicate using a software driven application program interface.

Please add the following claims.

22. The gaming machine of claim 10, wherein the first gaming processing subsystem board further comprises:

a serial UART (Universal Asynchronous Receiver/Transmitter).

C5

23. The gaming machine of claim 23, wherein the serial UART is used by the first gaming processing subsystem board to communicate with internal gaming devices, external gaming devices and combinations thereof.

24. The gaming machine of claim 10, wherein the first processing subsystem board further comprises:

a random number generator.

REMARKS

Claims 10-21 are currently pending in the application. Claims 10-21 were rejected. Claims 10, 11, 16 and 21 have been amended. Claims 12, 13, 14, 17, 18 and 19 have been cancelled. Claims 22, 23 and 24 have been added.

Rejections under 35 U.S.C. § 102

The examiner rejected claims 10-13, 15, 18 and 19 as being anticipated by Weiss (US Patent 6,071, 190.) Claims 10, 11 have been amended. Claims 12, 13, 18 and 19 have been cancelled. The rejection of claims 10, 11 and 15 as amended are respectively traversed.

The present invention, as described in claim 10, provides a hardware architecture for a gaming machine that is patentably distinct from the hardware architecture described in Weiss. In the present invention, gaming machine functionality is provided from a gaming processing subsystem board that may be connected to a motherboard on a PC-type personal computer (See 2nd and 3rd paragraph of Description of Embodiments). **Weiss does not teach a gaming processing subsystem board with this functionality (See the description below with respect**

to FIG. 6 in Weiss). Weiss and the present invention are described in more detail and compared in the following paragraphs.

In the present invention, as is well known in the computer arts, PC-type personal computers typically include a motherboard, a processor, a memory, expansion slots and various buses, such as a PCI bus. The expansion slots are used to connect boards or cards to the motherboard, such as a PCI expansion card. PC-type personal computers may be used perform multi-media functions, such as displaying graphics and sounds to a monitor connected to the computer. An advantage of the hardware architecture of the present invention is that it allows a PC architecture to be quickly adopted as a gaming machine platform (i.e., by adding the gaming processing subsystem board) and minimizes any custom or in-house non-standard work, such as software and hardware relating to improved graphics sound for general computing operations (See Page 4, 12-24 in specification).

In Weiss, the hardware architecture (see FIGs. 1, 6 and 7) is composed of a first processing area 20 and a second processing area 60 operatively coupled by via a communication link (See FIG. 1). The first processing area 20 is a "white box" that can be an interactive multi-media gaming computer (FIG. 7 and Col. 12, 1. 15-30). The first processing area 20 is used to provide multimedia gaming functions such as visual feedback to a gaming player (Col. 6, 1. 47-62). The present invention, as described in claim 10, comprises a motherboard with a first processor and a memory where "the first processor and the memory are designed or configured to control and operate one or more of i) visual displays, ii) attraction animation features, iii) audio player feedback, iv) real-time video presentations, v) and operating system and combinations thereof."

In Weiss, second processing area 60 is used to execute critical gaming functions (Col. 7, 1. 38-40). The critical gaming functions are stored in and executed directly from the read only memory 68 which is not alterable through any use of circuitry or programming of the gaming device (Col. 7, 1. 12-13). Critical functions include control of money handling devices, determining game outcome, progressive and bonus awards, random number generation, security events and historical logs (i.e., game history) (Col. 7, 1. 17-36). In the present invention, as described in claim 10, the first gaming processing board is "designed to control one or more of: i) a game play history, ii) gaming machine access, iii) user interface devices, iv) money handling devices, v) gaming machine I/O communications, v) random number generation and vi) progressive jackpot information."

In Weiss, the secure processing area 60, as described with respect to FIG. 6, includes a processor board 162, a main board 164 and a backplane 166 integrally or separately formed. The processor board 162 includes a graphics system processor 168 which is operatively coupled to the main board. The main board 164 includes the EPROM 68 and flash memory (as described in the previous paragraph, all of the critical gaming functions are executed from the EPROM 68). The main board 164 also includes a random number generator and a communication handler.

The main board allows for connections for a number of boards, such as a processor board 162, a video expansion board and a memory expansion board. The backplane 166 provides the coupling between the main board 164 and various input and output devices on the gaming machine. (FIG. 6 and Col. 11, 1. 33-45).

In contrast, the present invention, as described in claim 10, recites "a first gaming processing subsystem board connected to one of the buses on the motherboard, the first gaming processing subsystem board comprising; a) a second processor designed or configured to control the gaming machine and to control Input/Output to the gaming machine; b) a non-volatile memory for storing at least payout information; c) a data memory socket located on the first gaming processing subsystem board designed to accommodate a data prom; and d) a bus interface for connecting the first gaming processing subsystem board to one of the buses via one of the expansion slots on the motherboard." The first gaming processing subsystem board is designed to control one or more of: i) a game play history, ii) gaming machine access, iii) user interface devices, iv) money handling devices, v) gaming machine I/O communications, v) random number generation and vi) progressive jackpot information. The first gaming processing subsystem board is part of a gaming processing subsystem designed to control a game played on the gaming machine.

In Weiss, the elements of the game processing subsystem board of the present invention are distributed between the main board and other boards connected to the main board. In Weiss, the main board does not include a processor and processing is performed from a separate processor board. All of the critical gaming functions are stored in and executed directly from the read only memory 68, which is included on the main board. Also, the flash memory, which is a non-volatile memory, is located on the main board. Further, the communications handler is located on the main board. Weiss describes various boards connected to the main board. However, in Weiss, a gaming processing subsystem board with a processor, non-volatile memory and data memory socket that may be connected to the main board via an expansion slot on the main board and performs the gaming functions as described in claim 10 is not described. For at least these reasons, Weiss can't be said to anticipate the invention as recited in claims 10 and 11 and the rejection of these claims is believed overcome thereby.

Rejections under 35 U.S.C. § 103

The examiner rejected claims 14, 16, 17, 20 and 21 as being unpatentable over Weiss (US Patent 6,071, 190.) Claims 14, 17, 18 and 19 have been cancelled. The rejections of claims 16, 20, 21 as amended are respectively traversed. Claims 22-24 have been added.

Claims 16, 20, 21, 22, 23 and 24 provide additional patentably distinct limitations to claim 10. In Weiss, a motivation or suggestion for modifying the hardware architecture to provide the first gaming processor board of the present invention as described in claim 10 is not provided. In the present invention, the first gaming processor board is designed for compatibility

with a pc-type personal computer with multi-media functions. In Weiss, a multi-media gaming computer is provided but kept strictly separate from the gaming hardware that generates the critical gaming functions for security purposes. The gaming hardware and multi-media gaming computer each have separate main boards and expansion boards. Weiss teaches away from providing a gaming processing board of the present invention with the multi-media gaming computer in Weiss because it would compromise security. Thus, Weiss can't be said to render obvious claims 16, 20 and 21 and the rejection is believed overcome thereby.

Applicant believes that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP

David P. Olynick
Reg. No.: 48,615

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APPENDIX A

On page 5, 1st full paragraph, please substitute the following paragraph,

Figure 2 illustrates a gaming machine 30 that includes a housing 31, at least one user input 32 coupled to the housing, a display 33, such as, for example, a CRT, LCD or plasma display, coupled to the housing, a money input (for example, coin slot, bill validator, coupon acceptor, smart card reader, credit/debit card reader, or the other devices for accepting currency or credit), and a money output 35 (for example, coin chute, ticket printer, smart card writer, or other devices for issuing currency or credit). The gaming machine includes a control system [34] that includes processing platform 10 consisting of gaming processor subsystem and the general computing subsystem 11.

APPENDIX B

10. (Amended three Times) A gaming machine comprising:

a housing;

a user input connected to the housing;

a display connected to the housing; and

a control system located within the housing, the control system comprising a processing platform that comprises:

a mother board, said motherboard comprising;

a first processor;

a memory wherein the processor and the memory are designed or configured to control and operate one or more of i) visual displays, ii) attraction animation features, iii) audio player feedback, iv) real-time video presentations, v) and operating system and combinations thereof;

one or more buses on the more on the motherboard [a bus that uses]wherein each of the one or more bus uses an interface protocol selected from a group consisting of peripheral component interconnect (PCI), industrial standard architecture (ISA), Versa Module Europa (VME), and accelerated graphics port (AGP); and

one or more expansion slots for connecting a board to the buses; and

a gaming processing subsystem designed to control a game played on the gaming machine, the gaming processing subsystem comprising,

a first gaming processing subsystem board connected to the motherboard, the first gaming processing subsystem board comprising; [and]

a second processor designed or configured to control the gaming machine and to control Input/Output to the gaming machine;

a non-volatile memory for storing at least payout information;

a data memory socket located on the first gaming processing subsystem board designed to accommodate a data prom; and

a bus interface for connecting the first gaming processing subsystem board to [the bus] one of the buses via one of the expansion slots on the motherboard

wherein the first gaming processing subsystem board is designed to control one or more of: i) a game play history, ii) gaming machine access, iii) user interface devices, iv) money handling devices, v) gaming machine I/O communications, v) random number generation and vi) progressive jackpot information.[; and

a general computing subsystem designed to control audio presentations and video presentations on the gaming machine, the general computing subsystem comprising,

an expansion card;

a bus interface for connecting the expansion card to the bus.]

11. The gaming machine of claim 10, further comprising:

a second gaming processing subsystem board, said second gaming processing subsystem board comprising;.

12. Cancelled.

13. Cancelled.

14. Cancelled.

15. The gaming machine of claim 10, further comprising:

a serial communication connection.

16. The gaming machine of claim 10, wherein the gaming processor subsystem board is a PCI expansion card [and the bus is] designed to interface with a PCI bus.

17. Cancelled.

18. Cancelled.

19. Cancelled.

20. The gaming machine of claim 10, wherein the processing platform employs a personal computer processor architecture.

21. (Amended) The gaming machine of claim 10, wherein the [general computing subsystem] the first processor on the mother board and the first gaming processing subsystem board [gaming processor platform] communicate using a software driven application program interface.

22. The gaming machine of claim 10, wherein the first gaming processing subsystem board further comprises:

a serial UART (Universal Asynchronous Receiver/Transmitter).

23. The gaming machine of claim 23, wherein the serial UART is used by the first gaming processing subsystem board to communicate with internal gaming devices, external gaming devices and combinations thereof.

24. The gaming machine of claim 10, wherein the first processing subsystem board further comprises:

a random number generator.

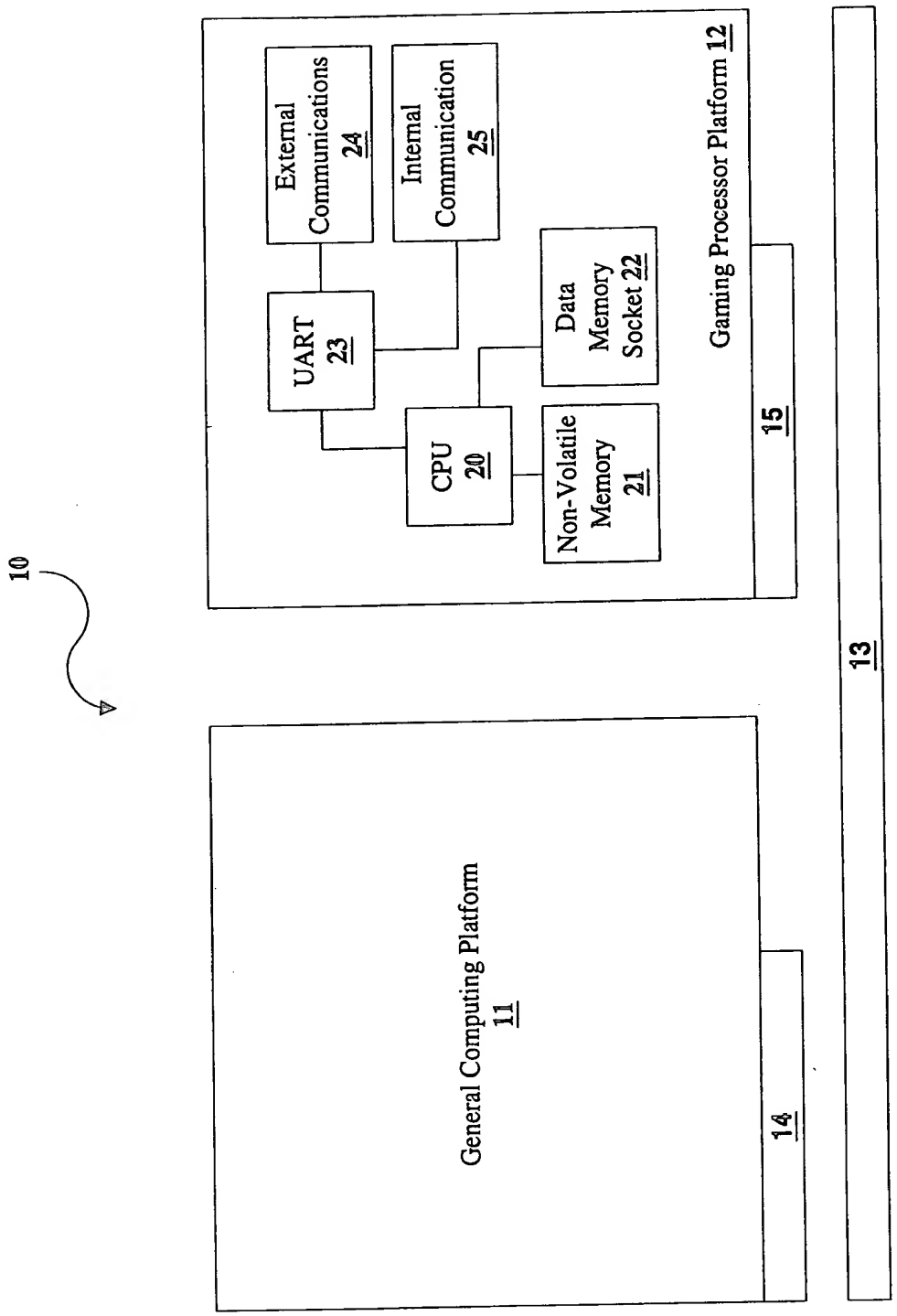
10
General Computing Platform
11
14
13
Gaming Processor Platform 12
15
External Communications 24
Internal Communication 25
UART 23
CPU 20
Non-Volatile Memory 21
Data Memory Socket 22

Figure 1

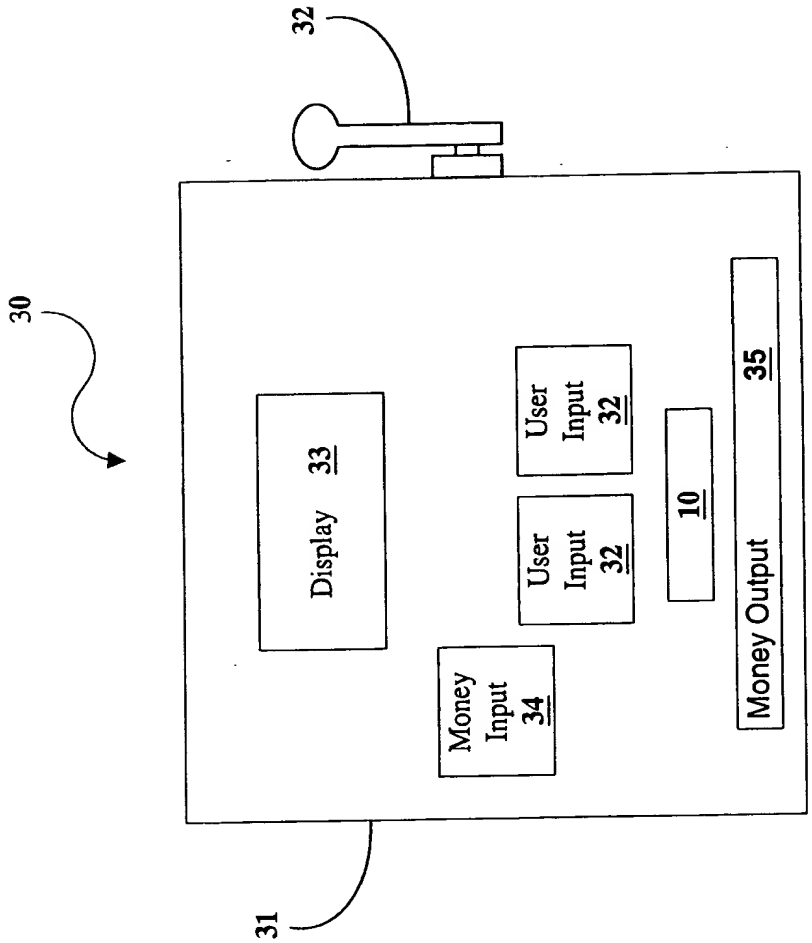
30
32
Display 33
User Input 32
User Input 32
10
Money Output 35
Money Input 34
31

Figure 2